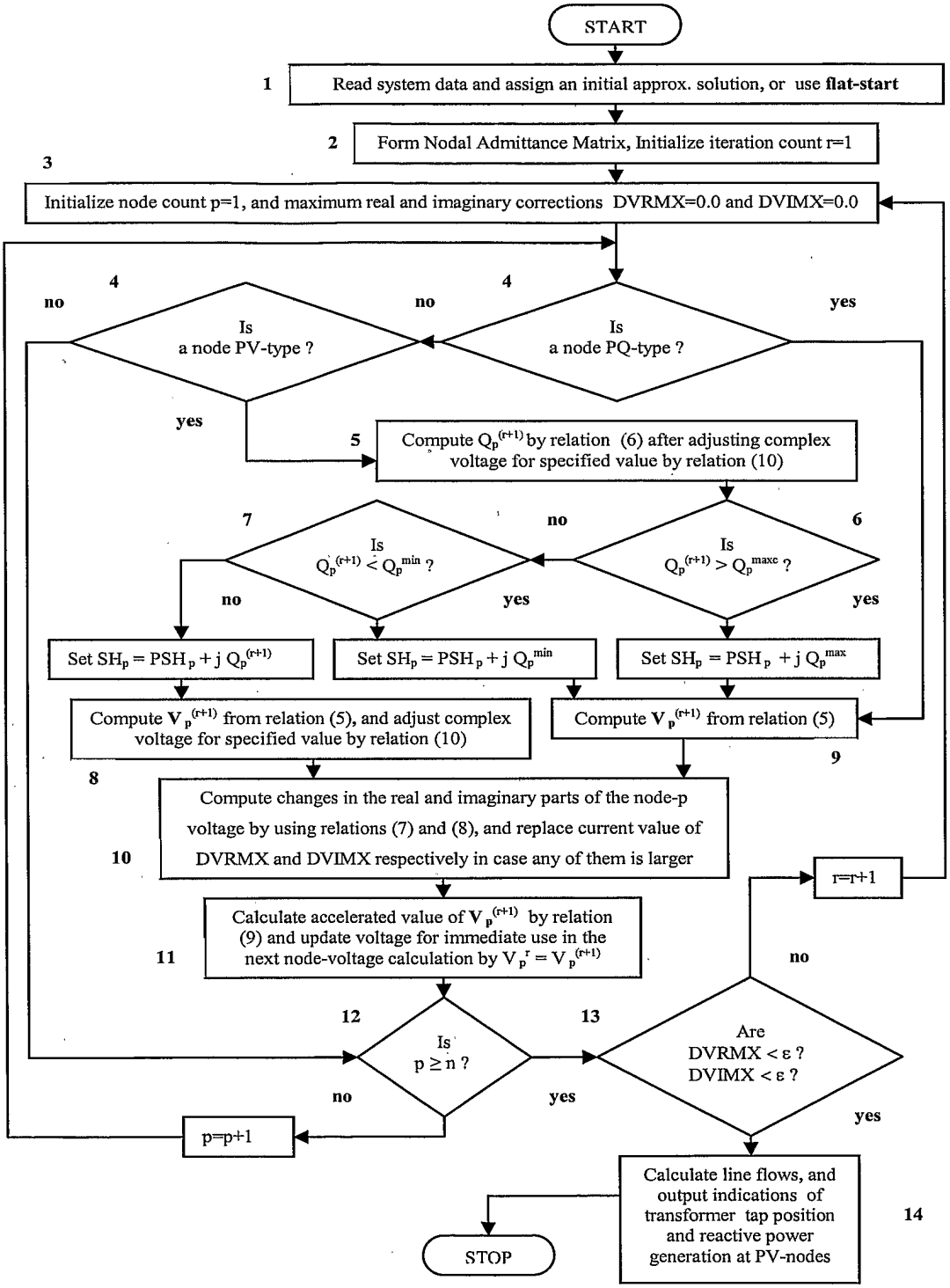

Fig. 1a: Prior Art: flow-chart of Gauss-Seidel Loadflow Algorithm-1a

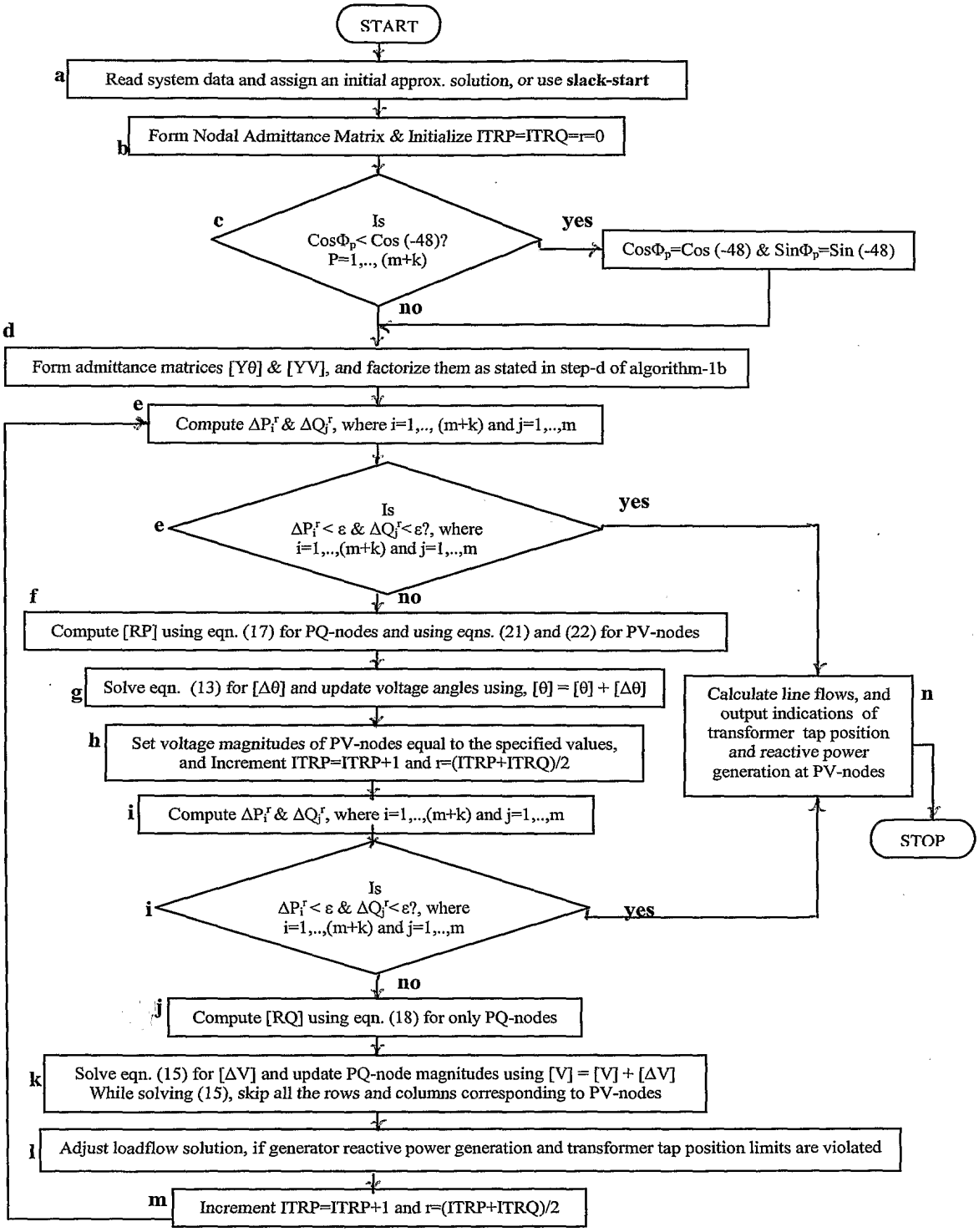

Fig.1b: Prior art: Flow-chart of SSDL solution algorithm-1b

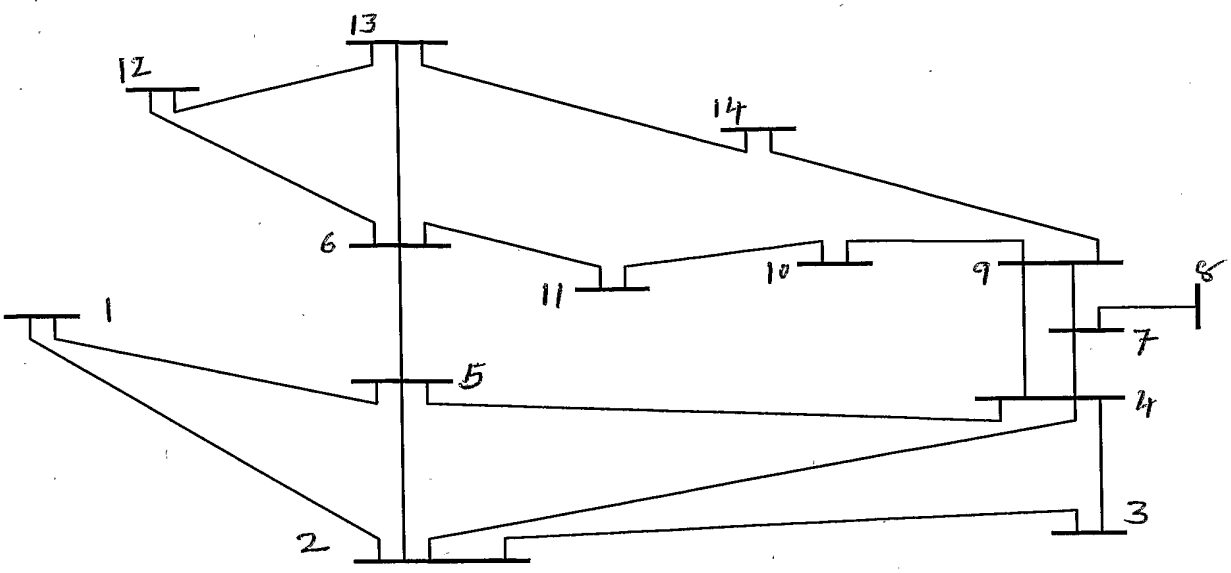

Fig. 2a: One-line diagram of IEEE 14-node network

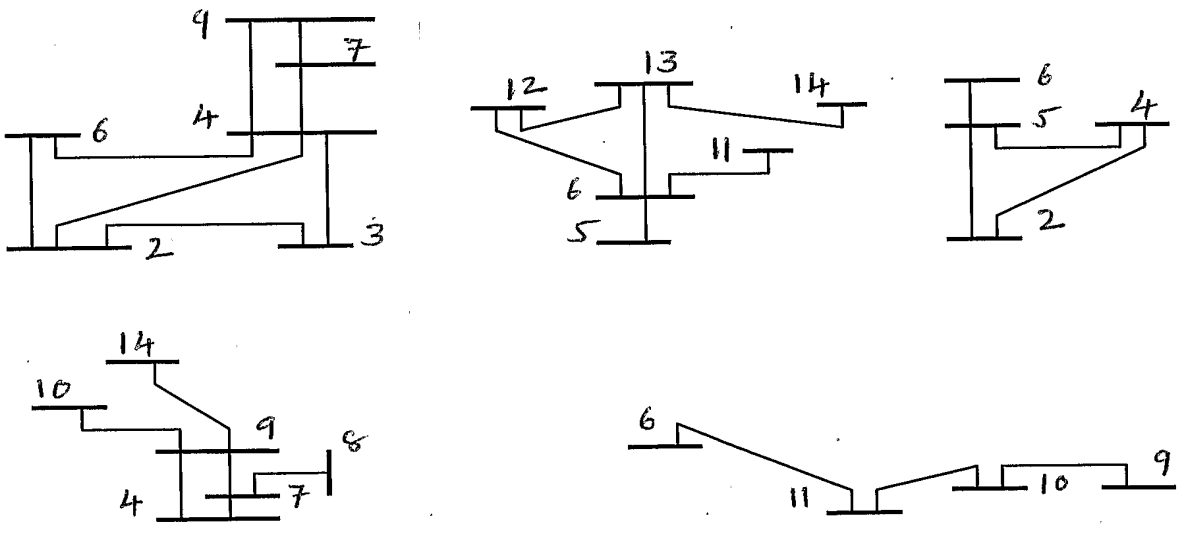

Fig. 2c: Non-redundant Level-1 sub-networks of fig. 2b are regrouped to reduce the number of processors required without increasing the number of nodes in any regrouped sub-network larger than the original largest sub-network of 6-nodes

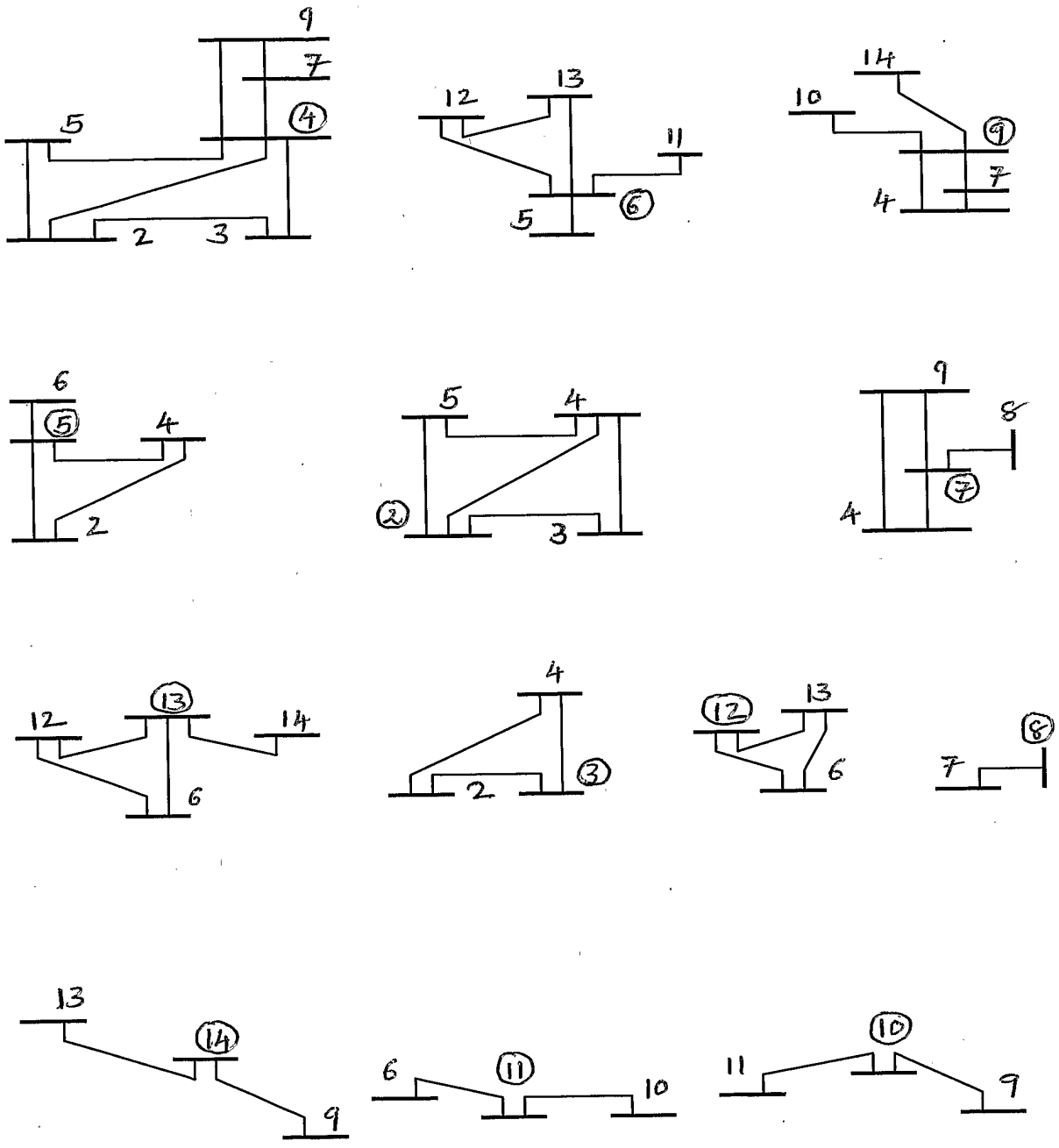

Fig. 2b: **Level-1 sub-networks around circled nodes for the network of fig. 2a**

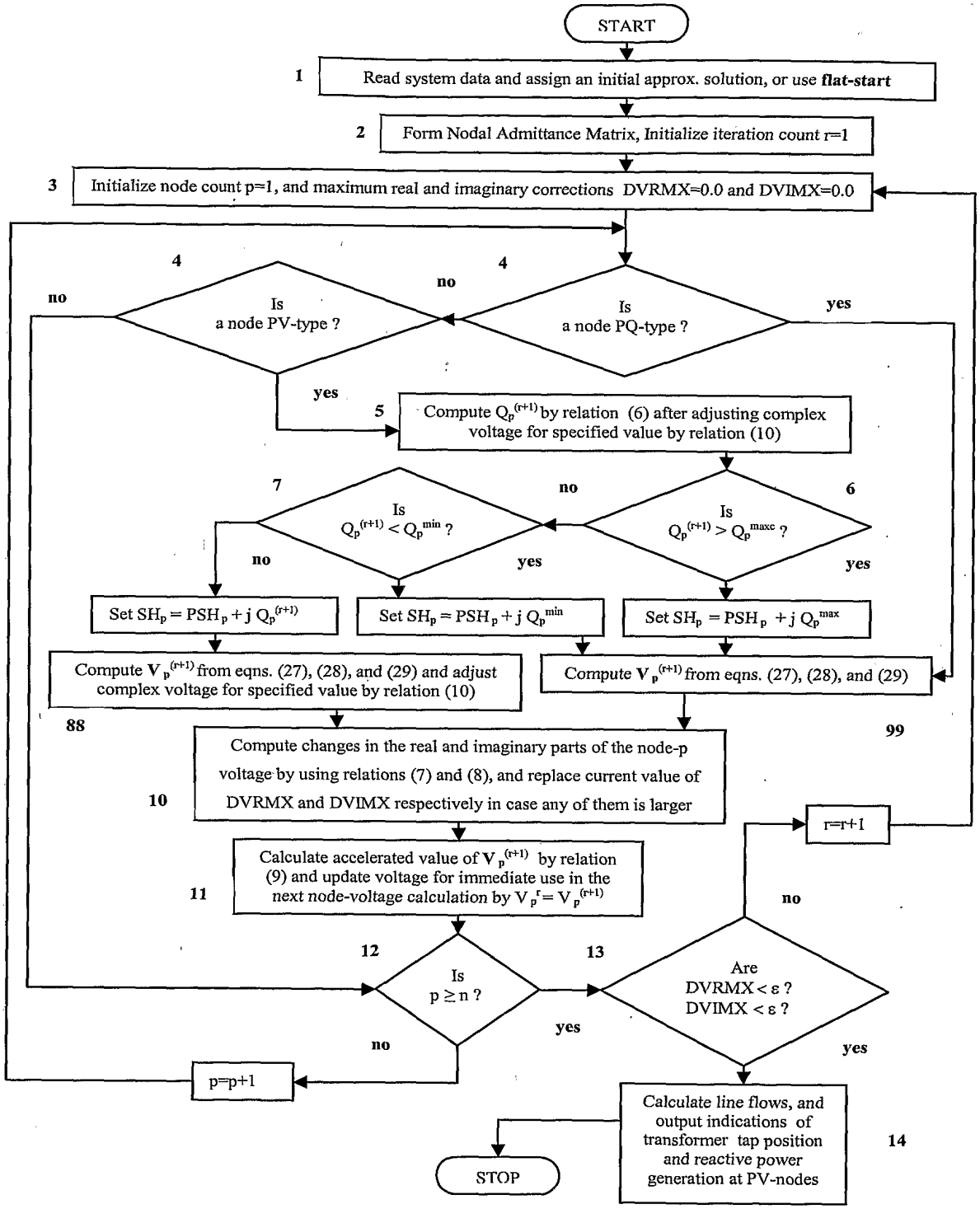

Fig. 3a: Invention: flow-chart of Gauss-Seidel-Patel Loadflow Algorithm-2a

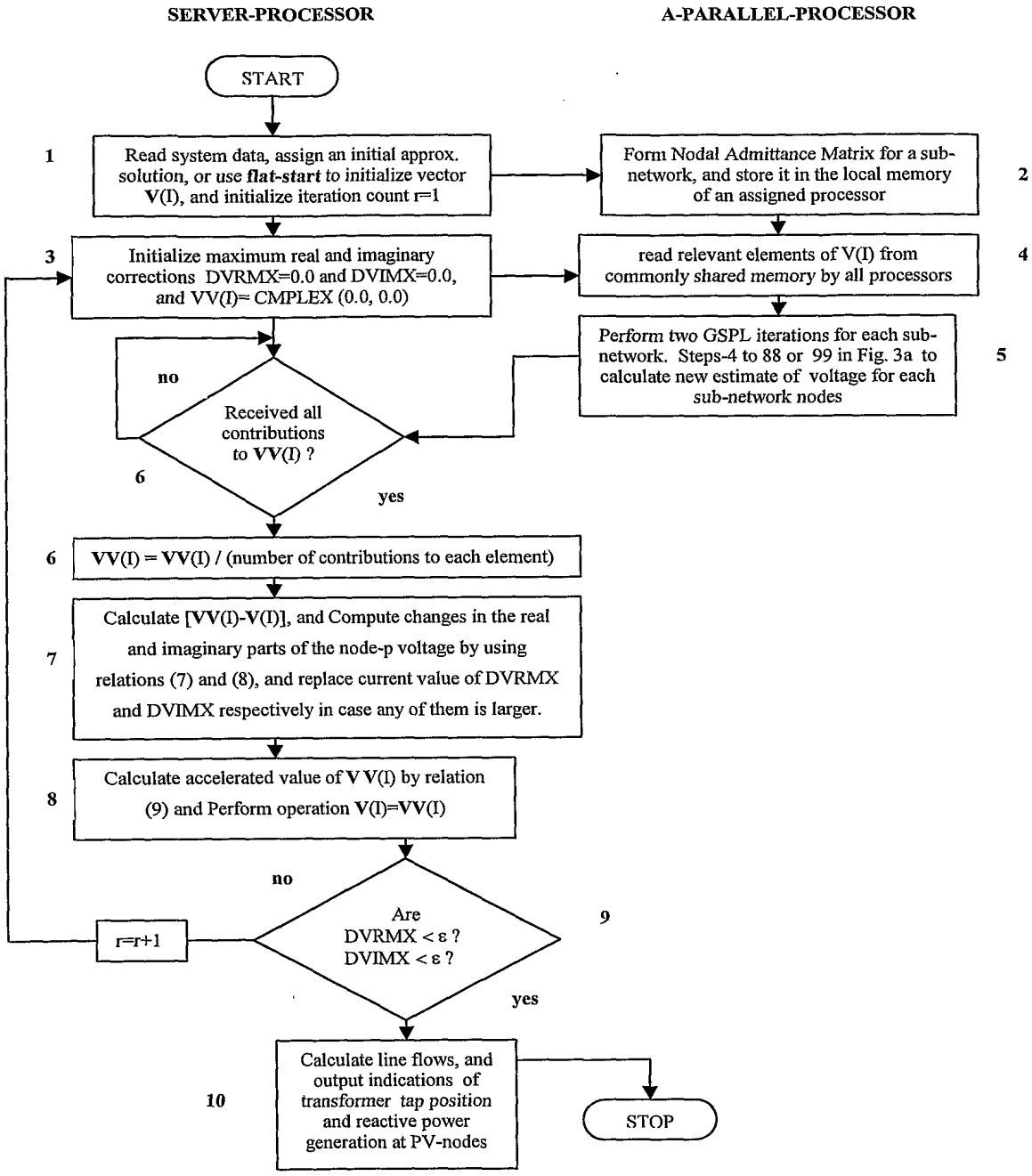

Fig. 3b: **Invention: flow-chart of Parallel-Gauss-Seidel-Patel Loadflow Algorithm-2b**

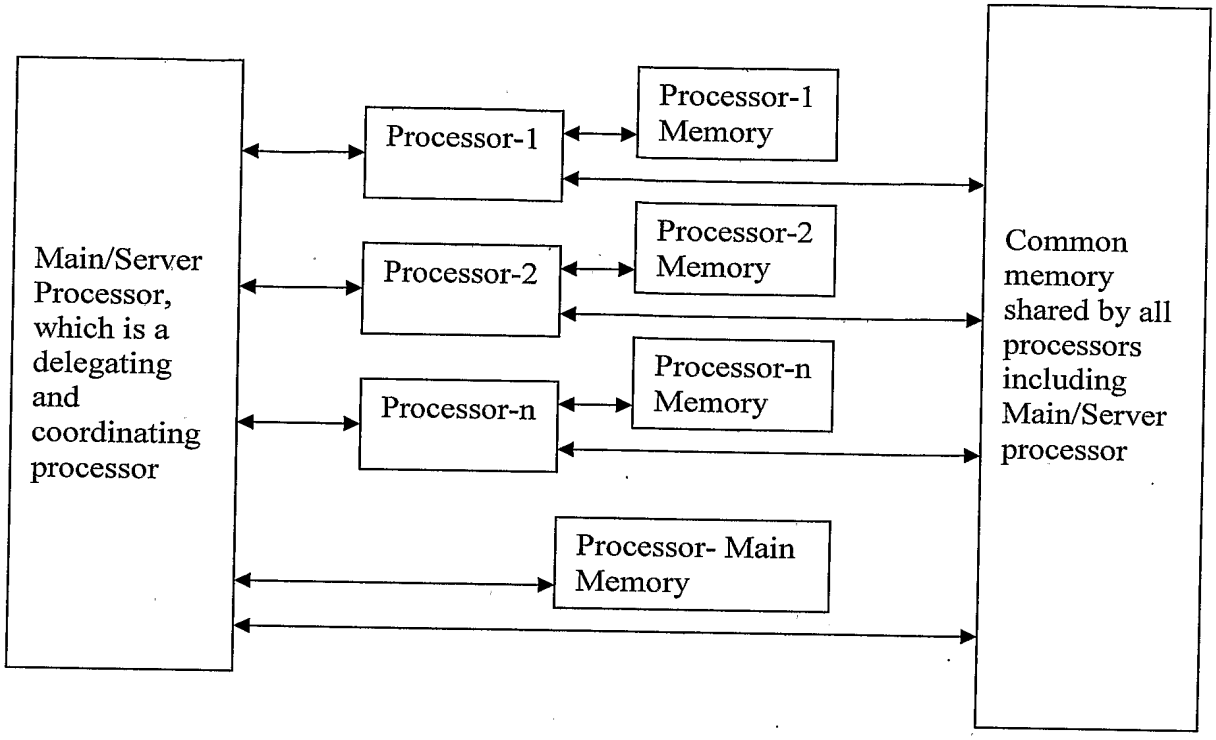

Fig. 4: Invented Parallel computer Architecture/organization

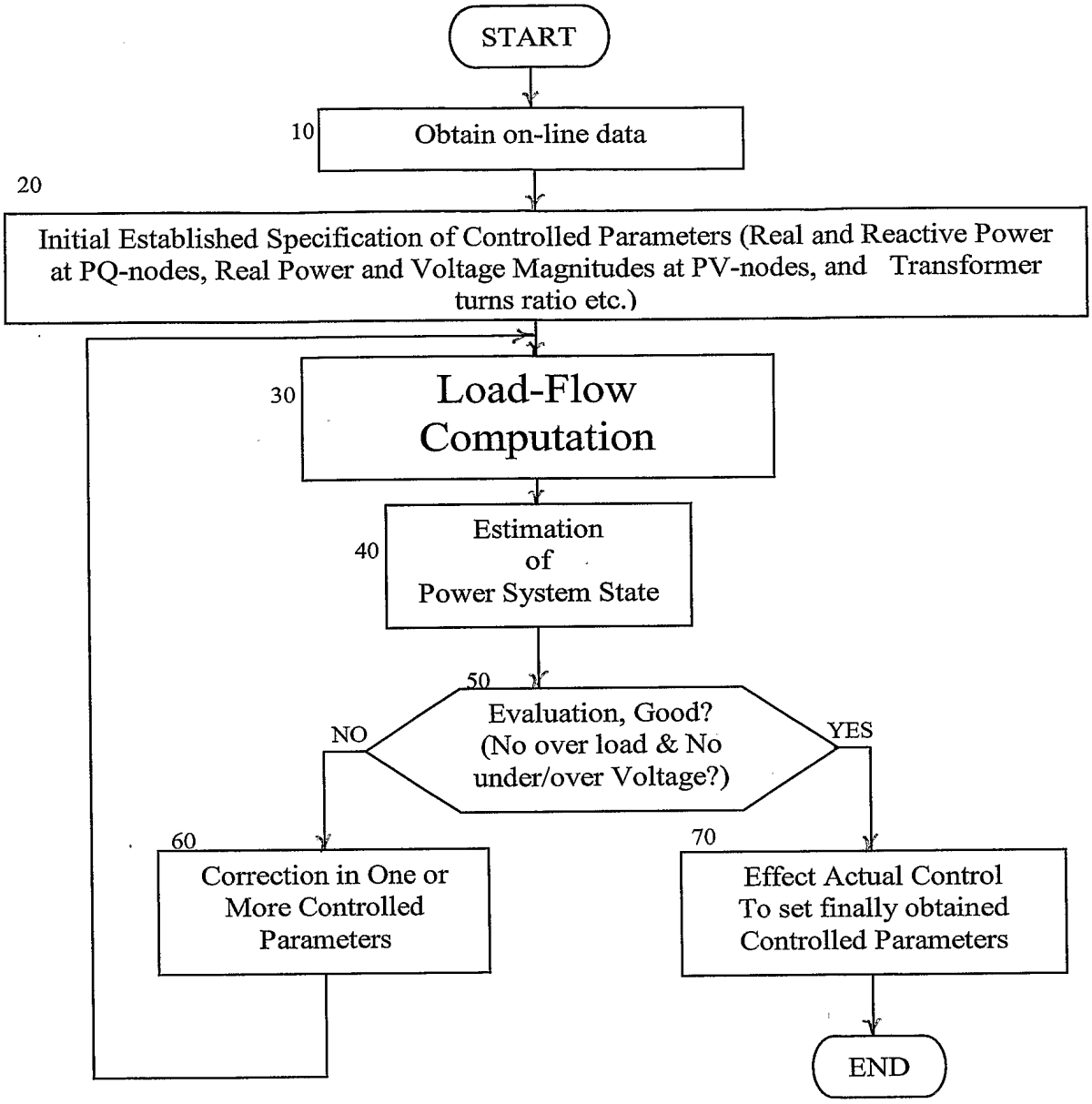

Fig. 5: Load-Flow Computation in Security Control of Electrical Power System (PRIOR ART)

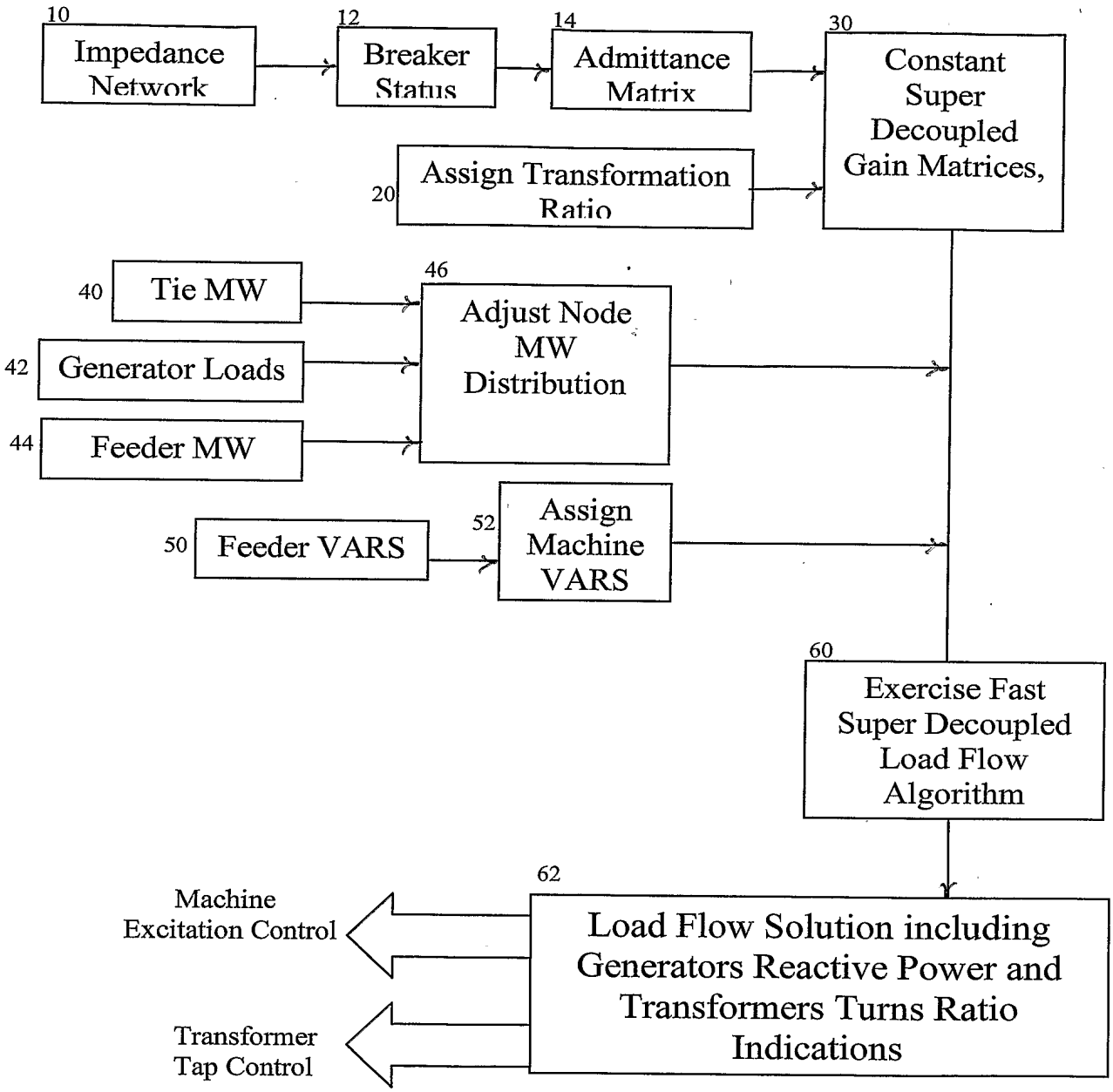

Fig. 6: Load-Flow Computation in Voltage Control of Electrical Power System (PRIOR ART)